must comprise:

- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit, wherein the first circuit directly combines the outputs of said at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array;

- such that the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, as amended, each pixel in the claimed photodetector array is an active pixel, which includes at least two photodiodes which are capable of being switched to a common pixel node (support for these amendments can be found with reference to FIGs. 2a and 2b). An array of "active" pixels is one which includes an amplifier for each pixel.

In addition, the array is arranged so that:

- the outputs of the at least two photodiodes making up a pixel can be combined in parallel, or

- the output of at least one of the pixel's two photodiodes can be combined with the photodiode of a neighboring pixel.

Each pixel in an array is "read out" to determine the amount of light which has impinged on the pixel. The amended claim 1 requires that the photodetector outputs be combined directly, prior to the pixel's being read out. This means that the

photodetector outputs themselves must be connected together ("combined") before the pixel is read out.

The cited art is quite different. The patent to Arques has almost no relevance whatsoever to the claims in question. Arques does disclose a pixel with two diodes, but this is the only similarity between the claimed array and Arques.

Arques discloses an array of passive pixels (i.e., no local amplifiers), each of which has one photosensitive diode and one reading diode (Abstract). Arques needs the second diode in order to read what he calls "the photosensitive dots". In this sense, the second diode is part of the readout circuitry and not related to the charge accumulation operation of the photodiode. The task of the second diode is to prevent the charge on the photosensitive dot from leaking out when reading other pixels in the same column. The two photodiodes in Arques' patent are connected in series with opposite directions of conduction (see title and FIG. 1 of his patent). This is required in order to perform the function he is describing: using the two diodes to read a specific photosensitive dot within a large array of pixels.

In all of these particulars, Arques differs radically from what is recited in the amended claim 1. In claim 1, all of the recited photodiodes may be involved in the charge accumulation operation; none of the photodiodes could be considered to be part of the readout circuitry.

In addition, claim 1 requires that the "at least two photodiodes [be] arranged such that their outputs are switchably connected to a common pixel node". See, for example, FIG. 2a, where the cathodes of photodiodes PD1 and PD2 in pixel 30 may both be connected to a common pixel node (by closing switch S1), and the cathodes of photodiodes PD3 and PD4 in pixel 32 may both be connected to a different common pixel node (by closing switch

S3).

The arrangement in Arques is very different. As noted in Arques' Abstract, each of his pixels consists of a photosensitive diode and a reading diode, connected in series between a row and a column of the matrix. As such, there is no way to connect the outputs of his diodes to a common pixel node - as is required in the amended claim 1.

Nor does Arques disclose anything remotely resembling the switching circuit and addressing circuit elements of claim 1. Arques says nothing about a means for "directly combining the outputs of said at least two photodiodes in parallel", or a means for "directly combining the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array" - as is required in claim 1. In fact, Arques says nothing about combining photodiode outputs in various combinations.

Nor does Arques disclose an array which is switchable between a high resolution and a low resolution pixel configuration, or an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, Arques fails to disclose the following elements of the amended claim 1:

- an array of active pixels;
- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;
- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit; wherein the first circuit directly combines the outputs of the at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one of the

photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby the array is switchable between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

In other words, the only property common to both claim 1 and Arques is the presence of 2 diodes. But the type of diodes, the way the diodes are connected, and the purpose and usage of the diodes are totally different - rendering the Arques patent largely irrelevant to the claims at issue.

The Examiner relies upon the patent to Wilder to make up for all the elements lacking in Arques, but Wilder does nothing to cure the deficiencies in Arques. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations.

It must first be noted that Wilder never even mentions photodiodes; his system is discussed at the pixel level only. This is in contrast to the applicant's invention, which focuses on the photodiode or photodiodes that make up each pixel. As noted above, claim 1 requires that the photodetector outputs be combined directly, which requires that the photodetector outputs be connected together before the pixel is read out. Because Wilder operates at the pixel level, he cannot and does not combine photodetector outputs prior to the pixel's being read out.

As such, Wilder cannot and does not disclose:

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit,

wherein the first circuit directly combines the outputs of said at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one photodiode in parallel with the output of a photodiode of a neighboring pixel in the array; nor

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Wilder's patent describes a way to achieve xy-addressability, but only for passive pixels; i.e., for pixels which lack a local amplifier. Simply, the charge on a pixel is read and then amplified externally; as such, it is very simple to change the resolution because one need only select more than one pixel at a time, and the charge of all selected pixels gets added on the read bus line or the external readout capacitor.

In contrast, the applicant's claim 1 recites an array of active pixels, with an amplifier for every pixel. The invention enables the effective resolution to be changed by connecting or isolating photodiodes before each pixel's readout amplifier.

To summarize, the combination of Arques and Wilder fails to disclose the following elements of the amended claim 1:

- an array of active pixels;

- at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

- a switching circuit which allows switching of at least one of the photodiodes between a first circuit and a second circuit; wherein the first circuit directly combines the outputs of the at least two photodiodes in parallel, and the second circuit directly combines the output of the at least one of the photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby the array is switchable

between a high resolution and a low resolution pixel configuration, the pixel having an intrinsic capacitance which stores the combined photodiode outputs prior to their being read out, and

- an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, virtually none of the elements of the amended claim 1 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would differ radically from the claimed array, in both structure and function.

As Arques and Wilder lack the above-noted essential elements of the amended claim 1, it is improper to find that claim 1 is obvious in view of them. The amended claim 1 is therefore allowable over Arques and Wilder.

Claim 5

The amended claim 1 is the parent of claim 5, which is therefore allowable along with claim 1.

Claim 9

Claim 9 is an independent claim directed to a photodetector array. Claim 9 has been amended in the same manner as was claim 1. As amended, claim 9 recites a photodetector array with selectable resolution, which comprises:

- a plurality of photodetectors;
- a switching circuit which configures neighboring photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, the photodetector outputs summed at each pixel arranged such that

their outputs are switchably connected to a common pixel node, the aggregated pixel output stored on the pixel's intrinsic capacitance prior to being read out;

- wherein the switching circuit is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

- a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of the pixel's to be read out in response to an address input.

Thus, as amended, each pixel in the claimed photodetector array is an active pixel, formed by aggregating photodetectors such that their outputs are summed together at a common pixel node.

In addition, the array is arranged so that:

- the switching circuit is electronically switchable between at least two different pixellization schemes with differing resolutions:

a first configuration in which each pixel output is a sum of two neighboring photodiodes; and

a second configuration in which each pixel output is a sum of at least three photodiodes.

As noted above, the cited art is quite different.

Arques discloses an array of passive pixels, made up of first and second diodes, with the second diode being part of the readout circuitry and not related to the charge accumulation

operation of the photodiode.

Furthermore, the two photodiodes in Arques' patent are connected in series with opposite directions of conduction. This is required in order to perform the function he is describing: using the two diodes to read a specific photosensitive dot within a large array of pixels.

In all of these particulars, Arques differs radically from what is recited in the amended claim 9. In claim 9, all of the recited photodetectors may be involved in the charge accumulation operation; none of the photodetectors could be considered to be part of the readout circuitry.

In addition, claim 9 requires that the photodetector outputs summed at each pixel are arranged such that their outputs are switchably connected to a common pixel node; this arrangement is shown, for example, in FIG. 2a, where the cathodes of photodiodes PD1 and PD2 in pixel 30 may both be connected to a common pixel node (by closing switch S1), and the cathodes of photodiodes PD3 and PD4 in pixel 32 may both be connected to a different common pixel node (by closing switch S3).

The arrangement in Arques is very different: each of his pixels consists of a photosensitive diode and a reading diode, connected in series between a row and a column of the matrix. As such, there is no way to connect the outputs of his diodes to a common pixel node in the manner specified in the amended claim 9.

Nor does Arques disclose anything remotely resembling the switching circuit and addressing circuit elements of claim 9. Arques says nothing about a means for providing "at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neigh-

boring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes" - as is required in claim 9. In fact, Arques says nothing about combining photodiode outputs in various combinations.

Nor does Arques disclose an addressing circuit which enables the combined photodiode outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

Thus, Arques fails to disclose the following elements of the amended claim 9:

- a switching circuit which configures neighboring photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output;

- photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node;

- wherein the switching circuit is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes.

In other words, both claim 9 and Arques require the use of multiple diodes. But the type of diodes, the way the diodes are connected, and the purpose and usage of the diodes are totally different - rendering the Arques patent largely irrelevant to the amended claim 9.

As noted above, the patent to Wilder does nothing to cure the deficiencies in Arques. Wilder discusses pixel addressing, but says nothing about combining photodiode outputs to achieve various pixel resolution configurations. Wilder never even mentions photodiodes; his system is discussed at the pixel level only. This is in contrast to the applicant's invention, which focuses on the photodiode or photodiodes that make up each pixel. As such, Wilder cannot and does not disclose:

- a switching circuit which is electronically switchable to aggregate the photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that the switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

- a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of the pixel's to be read out in response to an address input.

Wilder's patent describes a way to achieve xy-addressability, but only for passive pixels. In contrast, the applicant's claim 9 recites an array of active pixels, with an amplifier for every pixel. The invention enables the effective resolution to be changed by connecting or isolating photodiodes before each pixel's readout amplifier.

In sum, then, virtually none of the elements of the amended claim 9 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would be significantly different from the claimed array in both

structure and function.

As Arques and Wilder lack the above-noted essential elements of the amended claim 9, it is improper to find that claim 9 is obvious in view of them. The amended claim 9 is therefore allowable over Arques and Wilder.

Claim 15

Claim 15 is an independent claim directed to a photodetector array. Claim 15 has been amended in the same manner as were claims 1 and 9. As amended, claim 15 recites a photodetector array, comprising a plurality of active pixels comprising a plurality of pixels arranged into at least three horizontal rows and vertical columns,

- wherein each pixel comprises an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;
- and wherein the outputs of the subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations, wherein the at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column,
- each of the pixels having an intrinsic capacitance which stores the combined subpixel outputs prior to their being read out, and
- an addressing circuit which enables the combined subpixel outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

As above, the patent to Arques is largely irrelevant to the amended claim 15. Arques fails to disclose the following ele-

ments of the amended claim 15:

- an array of active pixels arranged into at least three horizontal rows and vertical columns;

- pixels which comprise at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;

- wherein the outputs of the subpixels are switchably combined into at least two different grouping arrangements to give at least two different selectable pixel configurations, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column.

As before, the patent to Wilder does nothing to cure the deficiencies in Arques. Wilder says nothing about combining subpixel outputs to achieve various pixel resolution configurations. As such, Wilder cannot and does not disclose:

- switchably combining the outputs of the subpixels into at least two different grouping arrangements, to give at least two different selectable pixel configurations, wherein the at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in the given vertical column, and

- an addressing circuit which enables the combined subpixel outputs stored on the pixel's intrinsic capacitance to be read out in response to an address input.

In sum, then, virtually none of the elements of the amended claim 15 are disclosed by the cited art - either alone or in combination. Even if combined as suggested, the resulting system would be significantly different from the claimed array in both

structure and function.

As Arques and Wilder lack the above-noted essential elements of the amended claim 15, it is improper to find that claim 15 is obvious in view of them. The amended claim 15 is therefore allowable over Arques and Wilder.

Claim 13-14

The amended claim 15 is the parent of claims 13-14, which are therefore allowable along with claim 15.

Claims 2 and 3 were rejected as obvious over Arques and Wilder in combination with a patent to Orava et al.

The amended claim 1 is the parent of claims 2 and 3, which are therefore allowable along with claim 1.

All of the claims presently in the application are believed to be in proper form for allowance. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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Attachment A:

Amended claims with insertions and deletions indicated.

1. (twice amended) A photodetector array comprising a plurality of addressable active pixels, each pixel comprising:

at least two photodiodes arranged such that their outputs may be switchably connected to a common pixel node;

a switching circuit which allows switching of at least one of said photodiodes between a first circuit and a second circuit;

wherein said first circuit directly combines the outputs of said at least two photodiodes in parallel, and said second circuit directly combines the output of said at least one of said photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby said array is switchable between a high resolution and a low resolution pixel configuration, said pixel having an intrinsic capacitance which stores said combined photodiode outputs prior to their being read out, and

an addressing circuit which enables the combined photodiode outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

9. (twice amended) A photodetector array with selectable resolution, comprising:

a plurality of photodetectors;

a switching circuit which configures neighboring ones of said photodetectors into active pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, said photodetector outputs summed at each pixel arranged such that their outputs are switchably connected to a common pixel node, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;

wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that said switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of two neighboring photodiodes; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

15. (twice amended) A photodetector array, comprising a plurality of <u>active</u> pixels, said array of pixels comprising a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein each pixel comprises an association of at least two subpixels <u>arranged such that their outputs may be switchably connected to a common pixel node</u>;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations, wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel

outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.